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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	3434.1US (97-856.1)
First Inventor or Application Identifier	Salman Akram
Title	A METHOD AND APPARATUS FOR FORMING METAL CONTACTS ON A SUBSTRATE
Express Mail Label No.	EL638949065US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

1. [X] * Fee Transmittal Form (e.g., PTO/SB/17) (Submit an original, and a duplicate for fee processing)
2. [X] Specification [Total Pages 21] (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings (if filed)
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) (35 U.S.C. 113) [Total Sheets 8]
4. Oath or Declaration [Total Pages 1]
   a. [ ] Newly executed (original or copy)
   b. [X] Copy from a prior application (37 C.F.R. § 1.63(d)) (for continuation/divisional with Box 17 completed) **[Note Box 5 below]**
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).
5. [X] Incorporation By Reference (useable if Box 4b is checked) The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program (Appendix)
7. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 C.F.R.§3.73(b) Statement (when there is an assignee) [ ] Power of Attorney
10. [ ] English Translation Document (if applicable)
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. [ ] * Small Entity Statement(s) (PTO/SB/09-12) [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. [ ] Other: ....

* A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.

17. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment:

[ ] Continuation [X] Divisional [ ] Continuation-in-part (CIP) of prior application No: 09 / 389,316

Prior application information: Examiner C. Arbes Group / Art Unit 3729

18. CORRESPONDENCE ADDRESS

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Signature	*James R. Duzan*	Date	11/08/2000

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FEE TRANSMITTAL for FY 2001

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($)1,088.00

Complete if Known	
Application Number	Not yet assigned
Filing Date	November 8, 2000
First Named Inventor	Salman Akram
Examiner Name	Unknown
Group Art Unit	Unknown
Attorney Docket No.	3434.1US (97-856.1)

METHOD OF PAYMENT

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

Deposit Account Number: 20-1469

Deposit Account Name: Trask Britt

[ ] Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

[ ] Applicant claims small entity status See 37 CFR 1.27

2. [X] **Payment Enclosed:**

[X] Check [ ] Credit card [ ] Money Order [ ] Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	710	201	355	Utility filing fee	710
106	320	206	160	Design filing fee	
107	490	207	245	Plant filing fee	
108	710	208	355	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 710.00

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims	41	-20** =	21	X	18	=	378
Independent Claims	3	- 3** =	0	X	80	=	0
Multiple Dependent					0	=	0

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	80	209	40	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 378.00

***or number previously paid, if greater; For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for *ex parte* reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	390	216	195	Extension for reply within second month	
117	890	217	445	Extension for reply within third month	
118	1,390	218	695	Extension for reply within fourth month	
128	1,890	228	945	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,240	241	620	Petition to revive - unintentional	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	710	246	355	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	710	249	355	For each additional invention to be examined (37 CFR § 1.129(b))	
179	710	279	355	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) ______________________

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) - 0 -

SUBMITTED BY				Complete *(if applicable)*	
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Signature	James R. Duzan			Date	11/08/2000

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NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EL638949065US

Date of Deposit with USPS: November 8, 2000

Person making Deposit: Amanda Trulson

APPLICATION FOR LETTERS PATENT

for

A METHOD AND APPARATUS FOR FORMING METAL CONTACTS ON A SUBSTRATE

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A METHOD AND APPARATUS FOR FORMING METAL CONTACTS ON A SUBSTRATE

CROSS-REFERENCE TO RELATED APPLICATION

This application is a divisional of application Serial No. 09/389,316, filed September 2, 1999, pending.

BACKGROUND OF THE INVENTION

The present invention relates generally to forming contacts on a semiconductor substrate and, more specifically, to the formation of metal bump contacts or connectors on a semiconductor substrate using micro-machining techniques.

Recent advances in data processing devices and memory circuits have resulted in the implementation of very large scale integrated circuits (VLSI) and even ultra large scale integrated circuits (ULSI). These VLSI and ULSI circuits are fabricated on semiconductor chips that include integrated circuits and other electrical parts. In order to mount a semiconductor chip to a carrier substrate, such as a printed circuit board or a ceramic substrate, solder bumps are arranged onto one of the semiconductor chip and the carrier substrate so that the semiconductor chip can be mechanically and electrically connected via metallurgical processes by melting the solder bumps.

One approach to applying and forming solder bumps and a carrier substrate is to use a solder paste. The solder paste is printed onto the carrier substrate and leads extending from the semiconductor chip are placed on the solder paste on the carrier substrate. The structure is then heated to cause the solder in the solder paste to melt so that the semiconductor chip can be mechanically and electrically connected to the carrier substrate. To place the solder paste onto the carrier substrate, a metal mask with predetermined openings is typically used. The solder paste is applied to the surface of the metal mask and a wiper is moved across the surface of the mask, thus pushing the solder paste through the openings of the metal mask onto the surface of the carrier substrate. Such masks are typically referred to as stencils.

Unfortunately, as the critical dimensions of the integrated circuits become smaller and smaller, the amount of solder paste that can be pressed through a given stencil becomes smaller and the placement of the solder paste becomes even more difficult. Additionally, with the smaller critical dimensions, the stencil mask becomes even more difficult to clean for a subsequent solder paste application as well as being subject to high rates of wear because of the constant placement of the stencil, application of the paste to the stencil, and removal and cleaning of the stencil.

Another method of placing conductive contacts for connecting the semiconductor chip to the carrier substrate has been to use preformed solder balls that are placed directly upon either the carrier substrate or the semiconductor chip with precisely controlled placement. Once the solder balls are in place, the solder balls are subjected to heat to cause a partial reflow so that the solder balls adhere to the solder pad. Unfortunately, in this process, as the critical dimensions of the features on the semiconductor chip tend to decrease, significant disadvantages become apparent in using this type of technique. One disadvantage is that the processing costs due to the limited process reliability and the speed of the pick and place nature of the transfer process become more evident. Another disadvantage is that the physical handling and placement of the solder balls by the machine dictates the minimum spacing allowed between solder bumps on a semiconductor chip or carrier substrate, and thus requires a semiconductor chip that would be larger than otherwise necessary for the desired VLSI or ULSI circuitry.

Additional problems involve the uniformity of the preformed solder balls. At smaller and smaller ball sizes, the average diameter of the preformed solder ball may vary greatly from the desired diameter of the preformed solder ball. This wide discrepancy in uniformity can lead to several problems. Preformed solder balls not only cannot applied where desired, but when a too large or too small preformed solder ball is placed upon a pad, after the formation of a connection using such a preformed solder ball, typically the location will be noted as either having several bad connections surrounding a ball that is too large or having a defective connection where a ball is too small. Large diameter preformed solder balls tend to prevent adjacent acceptable preformed solder balls from mechanically and electrically connecting between the carrier substrate and the semiconductor chip. Small diameter preformed solder balls are not large enough in diameter to connect to either of the two structures since the adjacent acceptable preformed solder balls are larger in diameter than the smaller ball, which can only touch one of the two surfaces.

Yet another technique has been developed that uses a method for forming solder balls on a semiconductor plate having apertures. One such technique is described in United States Patent 5,643,831, entitled "Process for Forming Solder Balls on a Plate Having Apertures Using Solder Paste and Transferring the Solder Ball to Semiconductor Device", issued July 1, 1997. The '831 Patent discloses a method for fabricating a semiconductor device using a solder ball forming plate having cavities. Solder paste is placed in the cavities using a solder paste application, such as a squeegee. Once the cavities are filled with solder paste, the solder ball forming plate is heated to form solder balls in the cavities while the plate is in an inclined position. The solder balls are then transferred from the plate to a semiconductor chip.

The solder ball forming plate is fabricated from a semiconductor material such as silicon, according to the following method. Initially, a substantially uniform flat surface is formed on the plate. Next, a plurality of cavities is formed in the flat surface of the plate. The cavities are formed by etching the semiconductor materials after a mask has been formed on the flat surface, each cavity having the shape of a precisely formed rhombus or parallelogram.

Yet another example of using a solder ball forming plate is disclosed in United States Patent 5,607,099, entitled "Solder Bump Transfer Device for Flip-Chip Integrated Circuit Devices", issued March 4, 1997. The '099 Patent discloses a carrier device that has cavities formed in its surface for receiving and retaining solder material. The solder material can then be transferred to a flip-chip as solder bumps. The cavities are located on the surface of the carrier device such that the location of the solder material corresponds to the desired solder bump locations on the flip-chip when the carrier device is placed in alignment with the flip chip. The size of the cavities can be controlled in order to deliver a precise quantity of solder material to the flip-chip. Further, in the '099 Patent, the apertures are fabricated so that they have a width of about 300 μm at the surface of the die and a width of about 125 μm at its base surface. Meanwhile, in the '831 Patent, the rhombus shaped cavities are design to produce a ball size of about 100 μm in diameter. Unfortunately, both of these structures cannot yet produce a ball size for a solder ball that approaches the dimensions currently required in placing a semiconductor chip upon a carrier substrate using the flip-chip technology. Additionally, the solder ball forming cavities are limited in shape.

Accordingly, it would be advantageous to overcome the problems of producing and using solder balls having uniform sizes as have been shown in the prior art approaches of utilizing preformed solder balls or to use metal masks or stencils to apply solder paste for reflow into solder balls. Additionally, it would be advantageous to make even smaller, more precisely formed solder balls than is possible in the prior art as well as to fabricate metal traces during the same step as that of forming solder balls using a solder ball forming plate.

Not only would it be advantageous to overcome the problems of producing uniform solder ball sizes for use in connecting a device to a substrate, but it would also be beneficial to provide a way of greatly improving the precision with which solder connections are made in alignment.

BRIEF SUMMARY OF THE INVENTION

According to the present invention, metal traces and solder bump pads are formed on a semiconductor substrate by way of a semiconductor template that has been micro-machined to receive solder paste material. The solder paste material is then formed into precisely-controlled ball shapes and metal trace geometries. First, a semiconductor substrate is covered with a mask material for protecting selected surfaces of the substrate that are not to be etched. Next, a mask is applied in order to anisotropically etch the substrate surface below. Solder ball sites and metal trace channels are formed at this time. A solder non-wettable material is applied to the exposed surfaces of the solder ball sites and the metal trace channels. A solder paste can then be applied uniformly across the surface of the substrate, thus filling in any sites and channels, or both, that are used to form the desired balls. The semiconductor template is then applied solder side to a second substrate so that the solder balls and traces can be applied directly on the second substrate, the solder balls being subsequently formed on the second substrate by the heating thereof to form the solder paste into a solder ball.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

FIGs. 1A-D illustrate a cross-sectional view of steps used in forming solder receiving holes and channels in a substrate mold according to the present invention;

FIG. 2 depicts a surface of the substrate mold having a plurality of cavities formed therein;

FIG. 3 illustrates the application of solder paste to the cavities and traces of the substrate mold of FIG. 2;

FIG. 4 depicts the formation of solder bumps in the first substrate mold as mated to a second substrate;

FIG. 5 depicts the second substrate having metal bumps and traces before final reflow;

FIG. 6 illustrates the formation of metal balls on the second substrate after reflow;

FIG. 7 illustrates a schematic diagram of a mold system using the solder mold according to the present invention;

FIG. 8 depicts a surface of a second embodiment of the substrate mold of the present invention having a plurality of hemispherical cross-sectional shaped cavities formed therein prior to the removal of the resist coating on the surface of the substrate mold;

FIG. 9 depicts the substrate mold of FIG. 8 having solder paste in the cavities formed therein in contact with a second substrate;

FIG. 10 depicts the second substrate having the solder paste applied thereto after the second embodiment of the substrate mold of the present invention of FIG. 8 is removed;

FIG. 11 depicts the second substrate of FIG. 10 after the solder paste has been heated to form solder balls on the second substrate;

FIG. 12 depicts a surface of a third embodiment of the substrate mold of the present invention having a plurality of rectangular cross-sectional shaped cavities formed therein;

FIG. 13 depicts the substrate mold of FIG. 12 having solder paste in the rectangular cavities in contact with a second substrate;

FIG. 14 depicts the second substrate of FIG. 13 having the rectangularly shaped solder paste thereon have been removed from the substrate of the third embodiment of the invention by the heating thereof;

FIG. 15 depicts the second substrate after the heating of the solder paste thereon to form solder balls;

FIG. 16 depicts a fourth embodiment of a substrate mold of the present invention having a plurality of cavities in a surface thereof and a plurality of heating elements on the other surface thereof;

FIG. 17 depicts the substrate mold of FIG. 16 having solder paste in the cavities formed in a surface thereof; and

FIG. 18 depicts the other side of the substrate mold of FIG. 16 illustrating the plurality of heating elements thereon along section line 18-18 of drawing Fig. 17.

DETAILED DESCRIPTION OF THE INVENTION

Illustrated in drawing FIGS. 1A-1D is a method for fabricating the semiconductor substrate to form metal bumps or metal traces, or both, on the surface of a secondary substrate. A semiconductor substrate, typically a flat planar substrate having a flat planar upper surface, a flat planar lower surface, and a plurality of planar sides forming the periphery of the substrate, is selected to serve as a bump forming substrate mold 10. The semiconductor substrate may be of any desired size and geometric shape suitable for use with an associated semiconductor device. The semiconductor substrate is selected from a semiconductor base material such as silicon, gallium arsenide, silicon on insulator, which may include silicon on glass or sapphire, or other well-known semiconductor substrate materials, as well as other similar types of materials, which are capable of being precisely micro-machined and having a coefficient of thermal expansion (CTE) similar to that of the semiconductor materials. In this particular application, it is preferred that a silicon substrate is used for substrate mold 10, although any of the other base materials may be freely substituted therefor. The silicon substrate is aligned such that the flat, planar upper surface 12 of substrate mold 10 defines the <100> plane of the substrate mold 10 which mates with a semiconductor device (not shown). As is shown in drawing Fig. 1A, a flat, planar upper surface 12 of substrate mold 10 has a first protective mask layer 14 located thereon. The mask layer 14 serves to protect the surface of substrate mold 10 when a subsequent etch schedule is performed to make the cavities or apertures in the flat, planar substrate surface 12. Mask layer 14 may be selected from particular etch resistant materials such as nitride, oxide, or a hardened polymer spin-on mask. Substrate mold 10 typically has a thickness of about 25 to 28 mils.

Next, in drawing FIG. 1B, a photoresist 16 is applied over the surface of mask layer 14 and then exposed through a mask to define openings exposing the selected cavity locations to be formed in surface 12. Then, as shown in FIG. 1C, a sufficient amount of semiconductor material is removed by an anisotropic etching from the exposed portion of the flat, planar surface 12 after penetration of the exposed portion of mask layer 14, thereby forming at least one cavity 18. Using an anisotropic etching process, the cavity 18 has walls sloped at 54° relative to the <100> plane of the substrate mold 10. The anisotropic etchant may be, for example, KOH, or other etchant materials well known to those skilled in the art. Further, if straight walls are desired, a dry etch using a plasma etch apparatus may be used to form cavity 18.

After the formation of cavity 18, mask layer 14 is removed using a dry-etch process that is selective to removing mask layer 14 only and not removing any of the underlying silicon either in the cavity 18 thus formed or on the flat, planar surface 12 of substrate mold 10. For example, if mask layer 14 is silicon dioxide, a removal substance such as phosphoric acid may be used. After the removal of the mask layer 14, a release layer 20 is formed over the entire surface 12 of substrate mold 10, particularly covering cavity 18. Release material 20 is selected from a material that is relatively non-wettable to metal solder. Such materials include silicon dioxide or silicon nitride, which can be applied using a chemical vapor deposition process. Other materials that are relatively non-wettable to metal solder may also be used, such as, for example, non-wettable polymers or the like. The result in structure is depicted in drawing FIG. 1D.

Although drawing FIGS. 1A-D illustrated only a single cavity 18, it is intended that a plurality of cavities be formed in an array across substrate mold 10. An example of a solder ball forming mold or substrate mold 10 that has such a plurality of cavities 18 is depicted in drawing FIG. 2. Release layer 20 is applied and utilized to minimize the wetting of solder paste on the substrate mold 10 when the assembly is heated in order to transfer the solder onto the bumps of the secondary surface.

Solder paste is applied, as shown in drawing FIG. 3, by use of an applicator 22, such as a squeegee, that is passed across the surface of substrate mold 10 pressing a metal solder paste 24 into the plurality of cavities 18 and wipes the excess paste away. The solder paste 24 fills cavities 18, thus forming frustroconically-shaped solder bumps 26 (shown in FIGS. 3 and 4).

Various types of metal solder may be used. The most widely employed types include a lead-tin combination. Other types of metal solder may include, but are not limited to, lead-silver, lead-tin-silver, lead-tin-indium, indium-tin, indium-lead, or any paste using copper or gold in combination with the lead or tin. For example, a lead-tin solder paste having a 63/37 weight ratio has a eutectic temperature of 183° C. Another type of lead-tin paste that has a 95/5 weight ratio has a eutectic temperature of about 350° C.

Once the solder paste 24 is applied to surface 12 of substrate mold 10, the entire assembly is heated to a temperature sufficient enough to slightly melt the metal solder paste in order to begin the formation of the solder bumps to be transferred. As shown in drawing FIG. 4, after this partially melted solder state has been reached, substrate mold 10 is inverted and applied to the surface of a carrier substrate 28, which may comprise a semiconductor device (die), wafer, or flexible substrate, such as a flex tape. The assembly of the substrate mold 10 and carrier substrate 28 is heated to a sufficient enough temperature to cause solder bumps 26 to slightly reflow and release from the release layer 20 formed on substrate mold 10. Substrate mold 10 is then removed and solder bumps 26 adhere to bond pads, terminal pads or other conductive, solder wettable sites 30 on carrier substrate 28, as shown in drawing FIG. 5. Next, an additional reflow step may be performed that causes solder bumps 26 to form into approximately spherically shaped solder balls 32 as attached to conductive sites 30 as depicted in drawing FIG. 6.

Because of the generally trapezoidal shape of solder bumps 26, the solder paste, upon heating reflow, draws into a substantially spherical shape and is held together by the surface tension of the solder material to form approximately spherically shaped solder ball 32 or a truncated spherical ball (not shown).

Although it has been depicted how solder balls or bumps 32 are formed in drawing FIG. 4, it is also possible to form metal traces using substrate mold 10. The same type of patterning and etch steps as described with respect to FIGS. 1A-1B would be followed, but would include a layout that would form metal traces or channels.

A solder mold system is depicted in drawing FIG. 7 which incorporates the substrate mold 10 shown in drawing FIGS. 1-6. The mold system includes solder applicator 22 for spreading metal paste 24 as dispensed by metal paste dispenser 52. Once the paste is sufficiently in place within the cavities 18, the substrate mold 10 is mated to a secondary substrate as shown in drawing FIG. 4, and then placed in a low-temperature metal paste reflow oven 54 to melt the paste to a sufficient enough consistency to form self-supported bumps and has sufficient enough tackiness to wet the conductive-gates on the carrier substrate 28.

Referring to drawing Fig. 8, an alternative embodiment of a substrate mold 40 of the present invention is illustrated. The substrate mold 40 is similar to the substrate mold 10 described hereinbefore as to construction and methods of construction except that the cavities 18 formed therein are hemispherically shaped. As illustrated, the mask layer 14 used to form the plurality of cavities 18 is present on portions of the flat planar upper surface 42 of the substrate mold 40. As with the substrate mold 10, the substrate mold 40 may include a release layer 20 to aid in the release of the solder paste contained within the hemispherical cavities 18.

Referring to drawing Fig. 9, once the solder paste 24 is applied to surface 42 of substrate mold 40 as described herein with respect to substrate mold 10 illustrated in drawing Fig. 3, the entire assembly of the substrate mold 40 and carrier substrate 28 having conductive sites or bond pads 30 located thereon for the solder paste 24 to be applied is heated to a temperature sufficient enough to slightly melt the metal solder paste 24 in order to begin the formation of the solder bumps to be transferred.

As shown in drawing FIG. 9, after this partially melted solder state has been reached, the assembly of the substrate mold 40 and the carrier substrate 28 is inverted so that the solder paste 24 in cavities 18 is applied to the conductive sites 30 on the surface of the carrier substrate 28, which may comprise a semiconductor device (die), wafer, or flexible substrate, such as a flex tape. The assembly of the substrate mold 40 and carrier substrate 28 is heated to a sufficiently high enough temperature to cause solder bumps 26 to slightly reflow and release from the release layer 20 formed on substrate mold 40. Substrate mold 40 is then removed and solder bumps 26 adhere to the conductive sites, bond pads, terminal pads or other conductive, solder wettable sites 30 on carrier substrate 28, as shown in drawing FIG. 10. Next, an additional reflow step may be performed that causes solder bumps 26 to form into approximately spherically shaped solder balls 32 attached to conductive sites 30 as depicted in drawing FIG. 11.

Because of the generally hemispherical shape of solder bumps 26, the solder paste, upon heating reflow, draws into a substantially spherical shape and is held together by the surface tension of the solder material to form approximately spherically shaped solder balls 32 or truncated spheres.

Referring to drawing Fig. 12, an alternative embodiment of a substrate mold 50 of the present invention is illustrated. The substrate mold 50 is similar to the substrate molds 10 and 40 described hereinbefore as to construction and methods of construction except that the cavities 18 formed therein are generally rectangular, or square shaped (shown in dashed lines). The mask layer 14 used to form the plurality of cavities 18 present on portions of the flat planar upper surface 42 of the substrate mold 50 is not illustrated. As with the substrate mold 10, the substrate mold 50 may include a release layer 20 to aid in the release of the solder paste contained within the hemispherical cavities 18. Referring to drawing Fig. 13, once the solder paste 24 is applied to surface 42 of substrate mold 50 as described herein with respect to substrate mold 10 illustrated in drawing Fig. 3, the entire assembly of the substrate mold 50 and carrier substrate 28 having conductive sites or bond pads 30 located thereon for the solder paste 24 to be applied is heated to a temperature sufficiently high enough to slightly melt the metal solder paste 24 in order to begin the formation of the solder bumps to be transferred.

As shown in drawing FIG. 13, after this partially melted solder state has been reached, the assembly of the substrate mold 50 and the carrier substrate 28 is inverted so that the solder paste 24 is applied to the conductive sites 30 on the surface of the a carrier substrate 28, which may comprise a semiconductor device (die), wafer, or flexible substrate, such as a flex tape. The assembly of the substrate mold 50 and carrier substrate 28 is heated to a sufficiently high enough temperature to cause solder bumps 26 to slightly reflow and release from the release layer 20 formed on substrate mold 50. Substrate mold 50 is then removed and solder bumps 26 adhere to the conductive sites, bond pads, terminal pads or other conductive, solder wettable sites 30 on carrier substrate 28, as shown in drawing FIG. 14. Next, an additional reflow step may be performed that causes solder bumps 26 to form into approximate spherically shaped solder balls 32 as attached to conductive sites 30 as depicted in drawing FIG. 15.

Because of the generally rectangular shape of solder bumps 26, the solder paste, upon heating reflow, draws into a substantially spherical shape and is held together by the surface tension of the solder material to form approximately spherically shaped solder balls 32.

Referring to drawing Fig. 16, another embodiment of the substrate mold 100 of the present invention is illustrated. The substrate mold 100 is similar to the substrate molds 10, 40, and 50 described hereinbefore. The substrate mold 100 includes cavities 18 having any desired shape as described herein in upper flat planar surface 12 and includes electrical resistance heating strips 66 located on the bottom thereof for the heating of the substrate mold 100 with electrical conductor 68 connected thereto. The bottom surface of the substrate mold 100 includes a coating 62 thereon to electrically insulate the heating strips 66 from the substrate mold 100. The heating strips 66 may be of any desired geometrical configuration to cover the bottom surface of the substrate mold 100 to uniformly heat the mold 100 and the solder paste 26 located in the cavities 18 thereof. The electrical conductor 68 may be any desired shape and have any desired location for connection to the heating strips 66. The electrical conductor 68 is covered with an insulation layer 70 located thereover. In areas or portions of the bottom surface of the substrate mold 100 not having a heating strip 66 located thereon, an insulative coating 64 of any suitable type is provided.

Referring to drawing Fig. 17, the substrate mold 100 is illustrated having solder paste 24 located in cavities 18 having release coating 20 therein. After the solder paste 24 is placed in the cavities 18, a carrier substrate 28 (see Fig. 4) is applied to the substrate mold 100, the assembly of the substrate mold 100 and carrier substrate 28 inverted, and the resistance heating strips 66 on the substrate mold 100 actuated to heat the solder paste 24 to transfer the same to the carrier substrate 28. After the solder paste 24 is transferred to the carrier substrate 28, the carrier substrate 28 is further heated to cause the solder paste to adhere to the conductive sites 30 on the carrier substrate 28 to substantially form solder balls 32 thereon.

Referring to drawing Fig. 18, the resistance heating strips 66 and conductor 68 are illustrated. The heating strips 66 may be of any desired shape to substantially uniformly heat the substrate mold 100. Similarly, the conductor 68 may be any desired shape to electrically connect to the heating strips 66. Further, any desired connector may be used to electrically connect the electrical conductor 68 to a source of electrical power.

Substrate molds 10, 40, 50 and 100 described herein are useful in forming contact bumps for many applications. One application is the formation of flexible connecting tape that requires bumps for interconnection of traces on the tape to a die or other element. The micro-machining of substrate mold 10 provides a much more accurate means for placing the solder ball shaped bumps over the prior art methods of merely placing bumps on top of a screen and then having the screen place the bumps in a proper alignment. Further, the solder ball shaped bumps have a more uniform volume and shape as the cavity dimensions in the semiconductor mold provide a substantially precise control over the formation of the solder ball shaped bumps. By contrast, in the prior art, the uniformity of solder balls has always been a problem, especially at the smaller diameter dimensions that are now being used. Another application for the present invention is for the direct placement of the solder ball shaped bumps on a semiconductor device or die for attachment. Yet another application includes placing the solder ball shaped bumps on a wafer-scale device for interconnection. This allows multiple devices placed on the same substrate to be interconnected using the precision of the solder ball shaped bumps. For example, the solder ball shaped bump application is useful in chip scale packages (CSP) or in fine ball grid array (FBGA) packages. The in situ resistance heating strip allows for selecting which balls need to be transferred by selectively heating only those resistance heating strips 66.

The applications of providing interconnect and bump contacts are numerous. For example, the metal trace interconnect and the bump contact may be used in any type of semiconductor device such as a memory storage device. These memory storage devices can range from read-only memory (ROM) and random access memory (RAM) to exotic types of memory such as video memory and the memory used in computer systems.

Additionally, the application of this metal trace interconnect and bump contact structure can be utilized in micro-processor packages that are used in computer systems as well as in other types of systems, and other types of single processing devices and support chips normally used in electronic devices. These electronic devices range from cellular phones to microwave systems, to automobiles and even programmable wrist watches.

Although the present invention has been described with reference to a particular embodiment, the invention is not limited to this described embodiment. The invention is limited only by the appended claims, which include within their scope all equivalent devices or methods which operate according to the principles of the invention as described.

CLAIMS

What is claimed is:

1. A mold apparatus for forming at least one metal bump for direct placement on bond pads on a secondary substrate, comprising:
a substrate having a surface;
at least one cavity formed in said surface of said substrate; and
a non-stick protective layer applied to said at least one cavity.

2. The mold apparatus according to claim 1, wherein said non-stick protective layer is a silicon oxide layer.

3. The mold apparatus according to claim 1, wherein said non-stick protective layer is a silicon nitride layer.

4. The mold apparatus according to claim 1, wherein said non-stick protective layer prevents metal material from adhering to said at least one cavity.

5. The mold apparatus according to claim 4, wherein said metal material is a solder paste comprising lead and nickel.

6. The mold apparatus according to claim 1, wherein said at least one cavity has a depth in said surface of said substrate of about 28 micrometers.

7. The mold apparatus according to claim 1, wherein said non-stick protective layer has a thickness ranging from about 200 Angstroms to 5 micrometers.

8. The mold apparatus according to claim 1, wherein said at least one cavity has a trapezoidal shape.

9. The mold apparatus according to claim 1, wherein said at least one cavity has a hemispherical shape.

10. The mold apparatus according to claim 1, wherein said at least one cavity has a rectangular shape.

11. The mold apparatus according to claim 1, wherein said at least one cavity has a square shape.

12. The mold apparatus according to claim 1, further comprising: at least one heating strip located on another surface of said substrate.

13. The mold apparatus according to claim 1, further comprising: a plurality of heating strips located on another surface of said substrate.

14. The mold apparatus according to claim 12, further comprising: an electrical conductor connected to a portion of the at least one heating strip.

15. The mold apparatus according to claim 13, further comprising: an electrical conductor connected to a portion of the plurality of heating strips.

16. The mold apparatus according to claim 1, wherein said substrate comprises semiconductor material.

17. The mold apparatus according to claim 1, wherein said substrate comprises ceramic material.

18. A solder mold apparatus for forming at least one metal bump for direct placement on a corresponding bond pad on a secondary substrate, comprising:

a substrate having a surface;
at least one cavity formed in said surface of said substrate;
a non-stick protective layer applied to said at least one cavity; and
a metal paste applicator.

19. The solder mold apparatus according to claim 18, wherein said non-stick protective layer is a silicon oxide layer.

20. The solder mold apparatus according to claim 18, wherein said non-stick protective layer is a silicon nitride layer.

21. The solder mold apparatus according to claim 18, wherein said non-stick protective layer prevents metal material from adhering to said at least one cavity.

22. The solder mold apparatus according to claim 21, wherein said metal material is a solder paste comprising lead and nickel.

23. The solder mold apparatus according to claim 22, further comprising a metal paste dispenser, coupled to said metal paste applicator, to place a metal paste on said substrate.

24. The solder mold apparatus according to claim 23, further comprising a heating element to melt said metal paste to form a contact for application to said secondary substrate.

25. The solder mold apparatus according to claim 18, wherein said at least one cavity has a depth in said surface of said substrate of about 28 micrometers.

26. The solder mold apparatus according to claim 18, wherein said non-stick protective layer has a thickness ranging from 200 Angstroms to 5 micrometers.

27. The solder mold apparatus according to claim 18, wherein said substrate comprises semiconductor material.

28. The solder mold apparatus according to claim 18, wherein said substrate comprises a ceramic material.

29. A mold apparatus for forming at least one metal bump for direct placement on bond pads on a secondary substrate, comprising:

a substrate having a surface;

at least one cavity formed in said surface of said substrate, said at least one cavity having a selected width and a selected length in said surface; and

a non-stick protective layer applied to said at least one cavity.

30. The mold apparatus according to claim 29, wherein said non-stick protective layer is a silicon oxide layer.

31. The mold apparatus according to claim 29, wherein said non-stick protective layer is a silicon nitride layer.

32. The mold apparatus according to claim 29, wherein said non-stick protective layer prevents metal material from adhering to said at least one cavity.

33. The mold apparatus according to claim 32, wherein said metal material is a solder paste comprising lead and nickel.

34. The mold apparatus according to claim 29, wherein said at least one cavity has a depth in said surface of said substrate of about 28 micrometers.

35. The mold apparatus according to claim 29, wherein said non-stick protective layer has a thickness ranging from about 200 Angstroms to 5 micrometers.

36. The mold apparatus according to claim 29, wherein said selected width and said selected length are substantially the same.

37. The mold apparatus according to claim 29, wherein said selected width is smaller than said selected length.

38. The mold apparatus according to claim 29, wherein said at least one metal bump has substantially the same dimensions as said at least one cavity.

39. The mold apparatus according to claim 29, further comprising: at least one heating strip located on another surface of said substrate.

40. The mold apparatus according to claim 29, further comprising: a plurality of heating strips located on another surface of said substrate.

41. The mold apparatus according to claim 29, wherein said substrate comprises semiconductor material.

ABSTRACT OF THE DISCLOSURE

Metal traces and solder bump pads are formed on a semiconductor substrate by way of a semiconductor template that has been micro-machined to receive solder paste material. The solder paste material is then formed into precisely-controlled ball shapes and metal trace geometries. First, a semiconductor substrate is covered with a mask material for protecting selected surfaces of the substrate that are not to be etched. Next, a mask is applied in order to etch the substrate surface below. Solder ball sites and metal trace channels are formed at this time. A solder non-wettable material is applied to the exposed surfaces of the solder ball sites and the metal trace channels. A solder paste can then be applied uniformly across the surface of the substrate, thus filling in any sites and channels, or both, that are used to form the balls in metal traces desired. The semiconductor template is then applied solder side to a second substrate so that the solder balls and traces can be applied directly on the second substrate using heat to reflow the solder to the second substrate.

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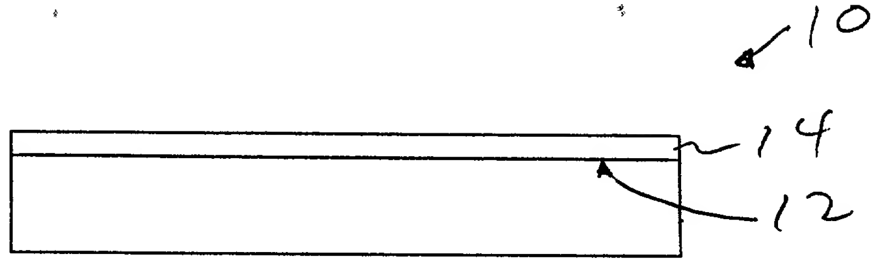

FIG. 1A

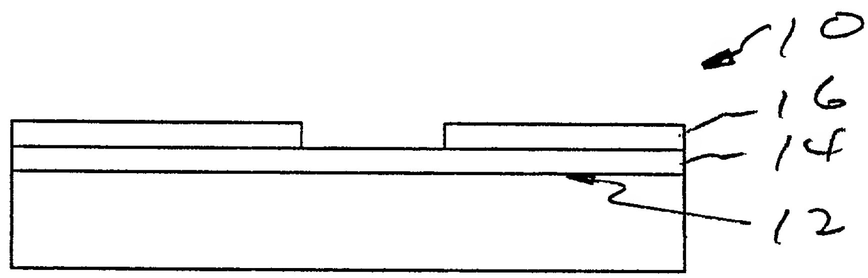

FIG. 1B

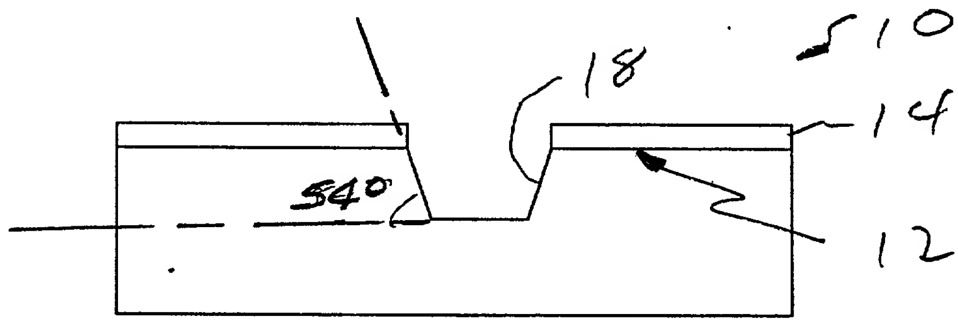

FIG. 1C

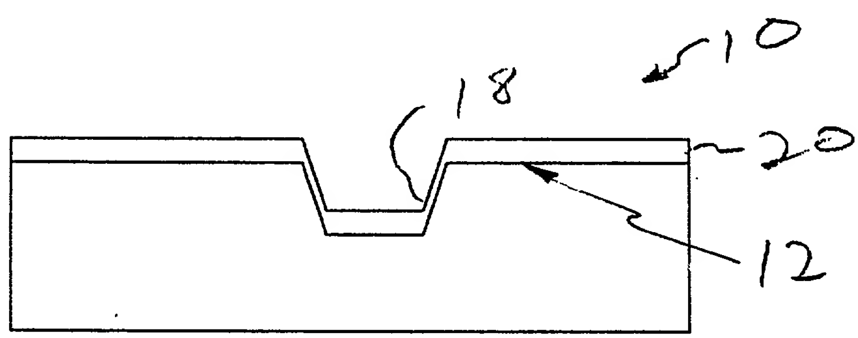

FIG. 1D

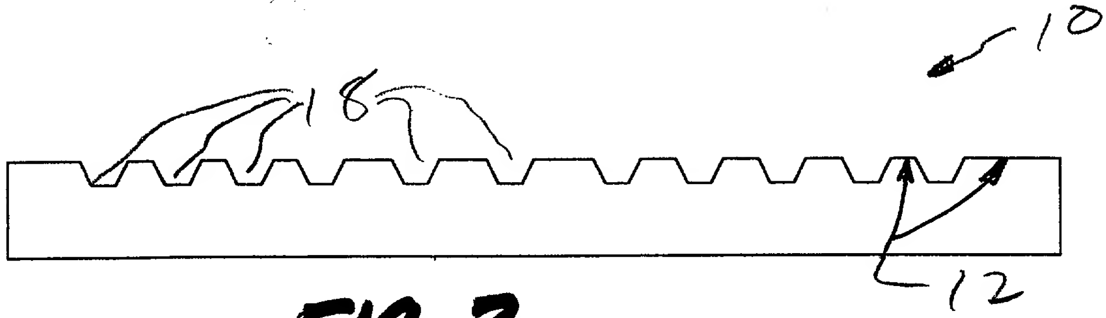

FIG. 2

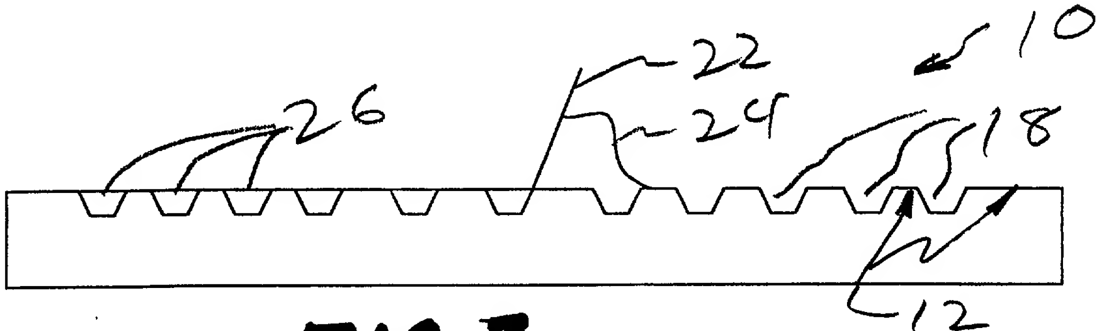

FIG. 3

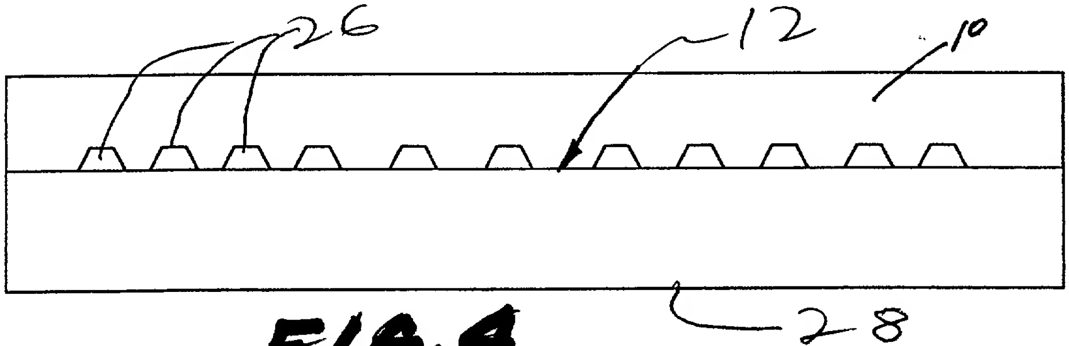

FIG. 4

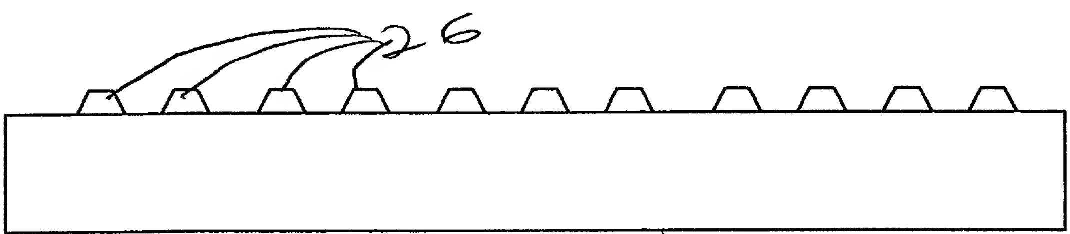

FIG. 5

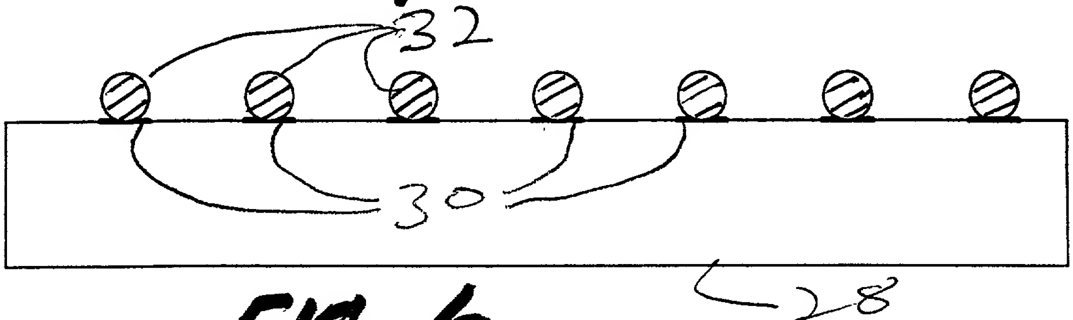

FIG. 6

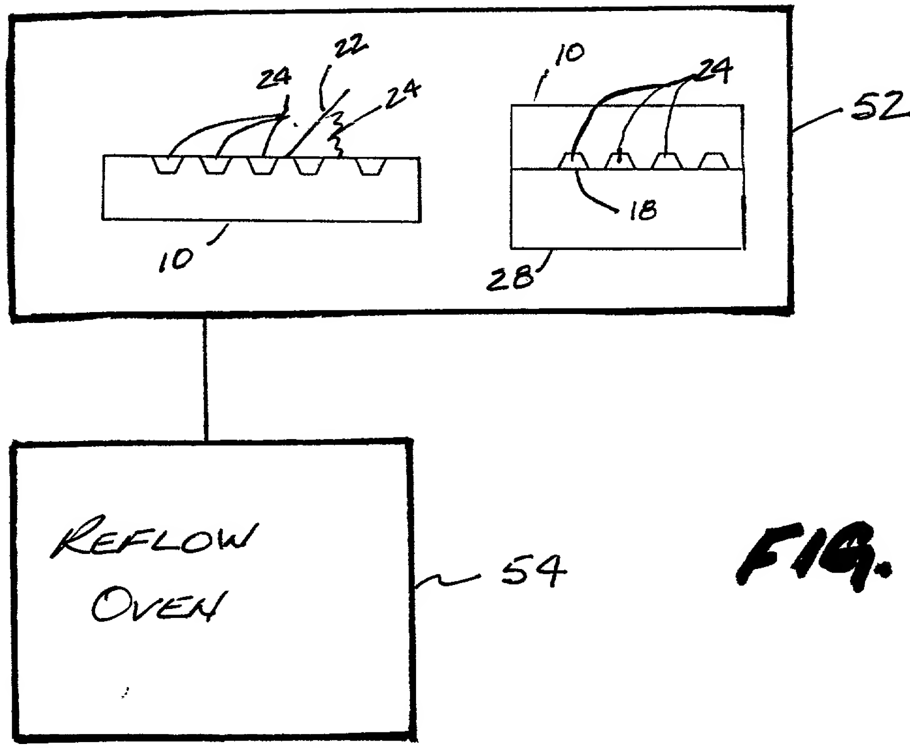

FIG. 7

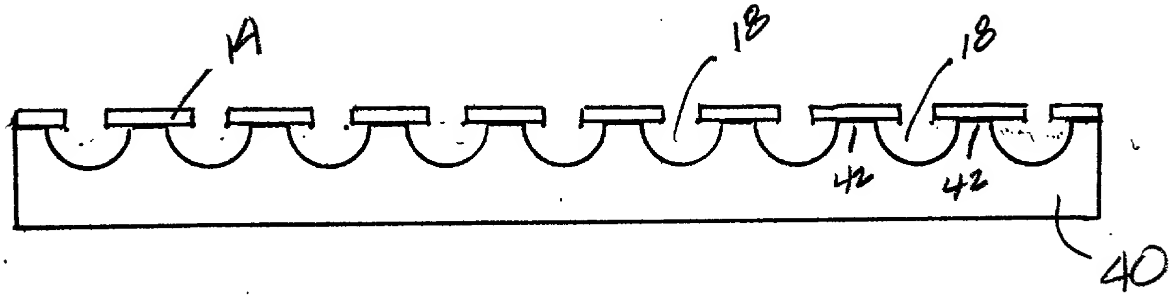

FIG. 8

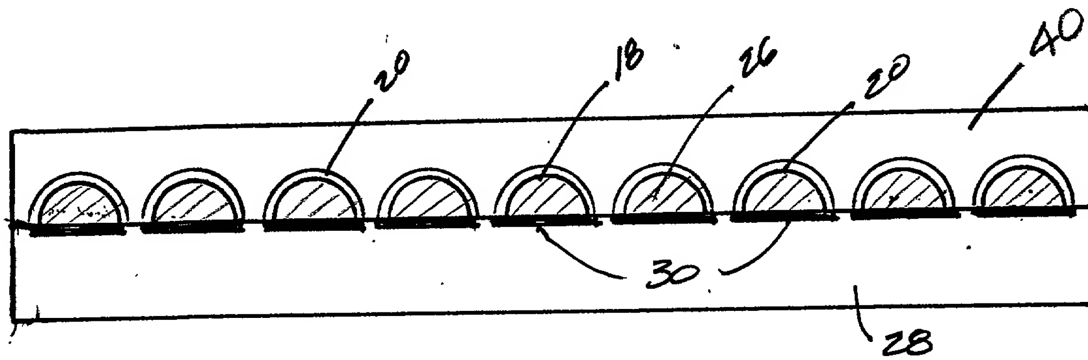

FIG. 9

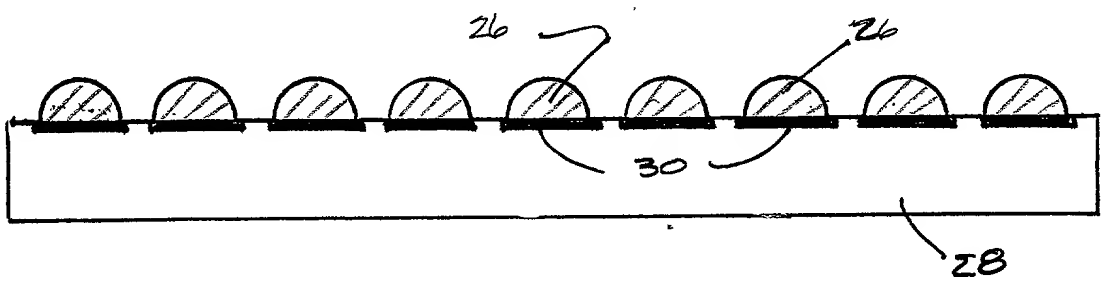

FIG. 10

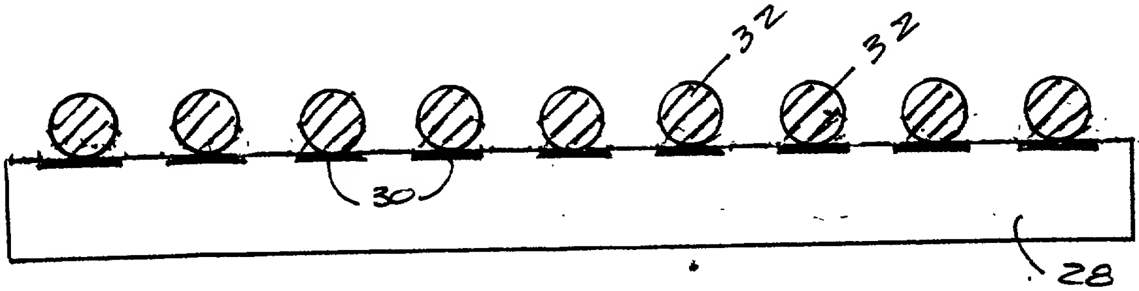

FIG. 11

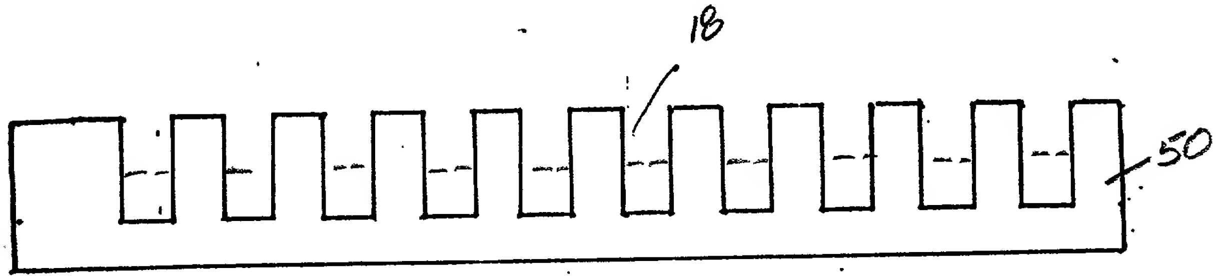

FIG. 12

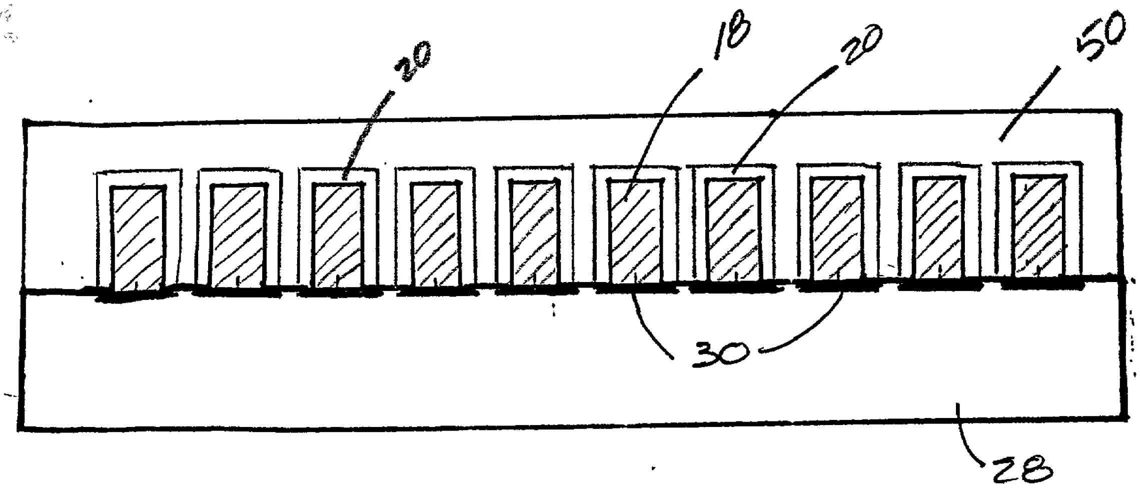

FIG. 13

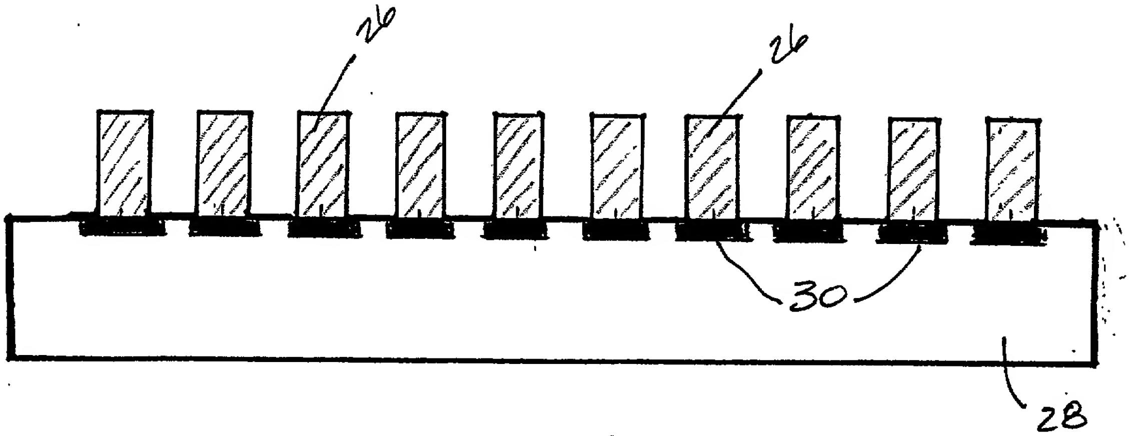

FIG. 14

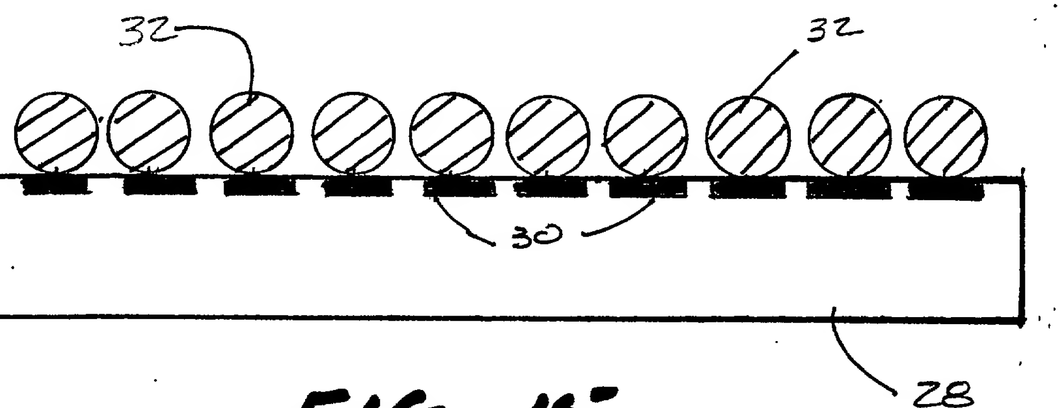

FIG. 15

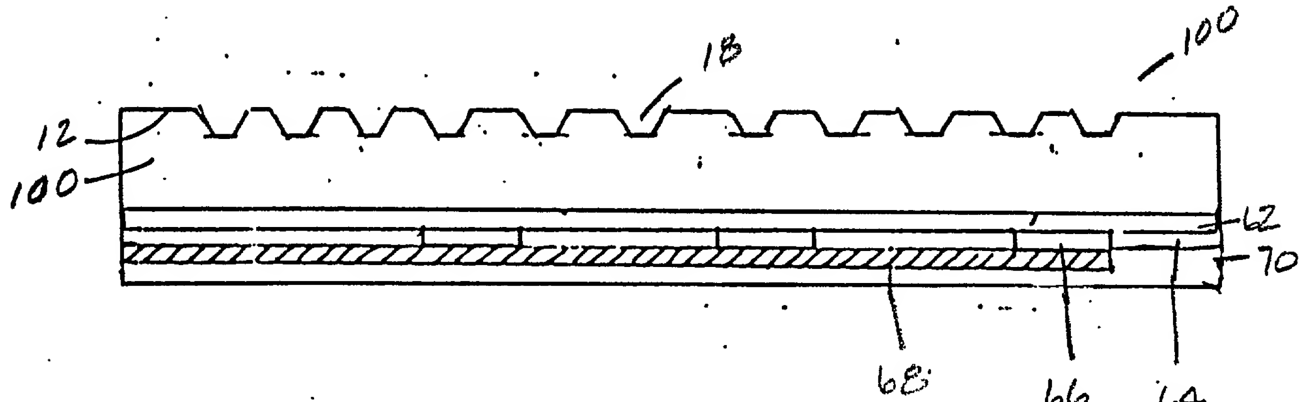

FIG. 16

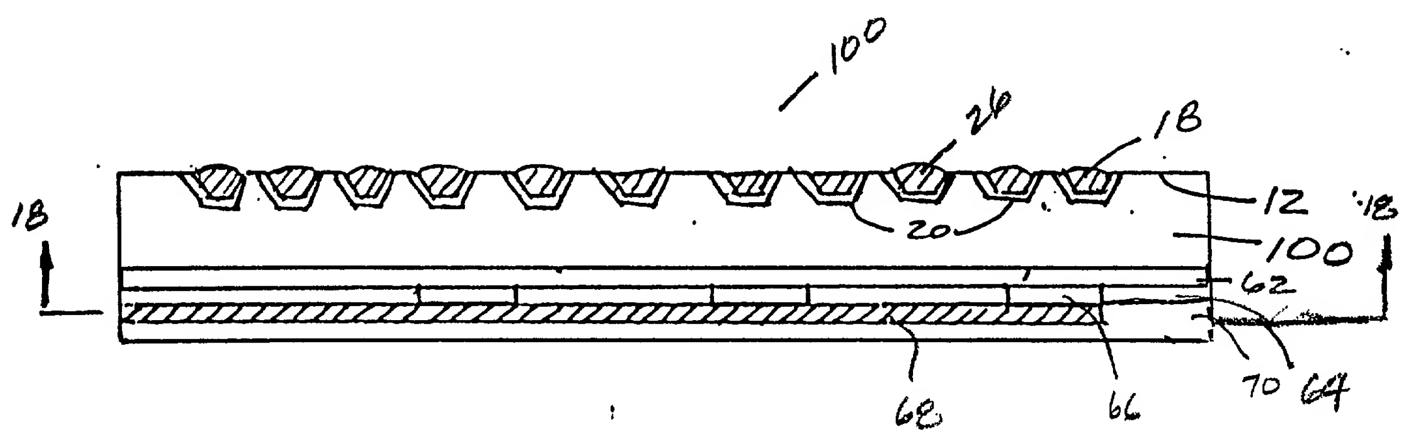

FIG. 17

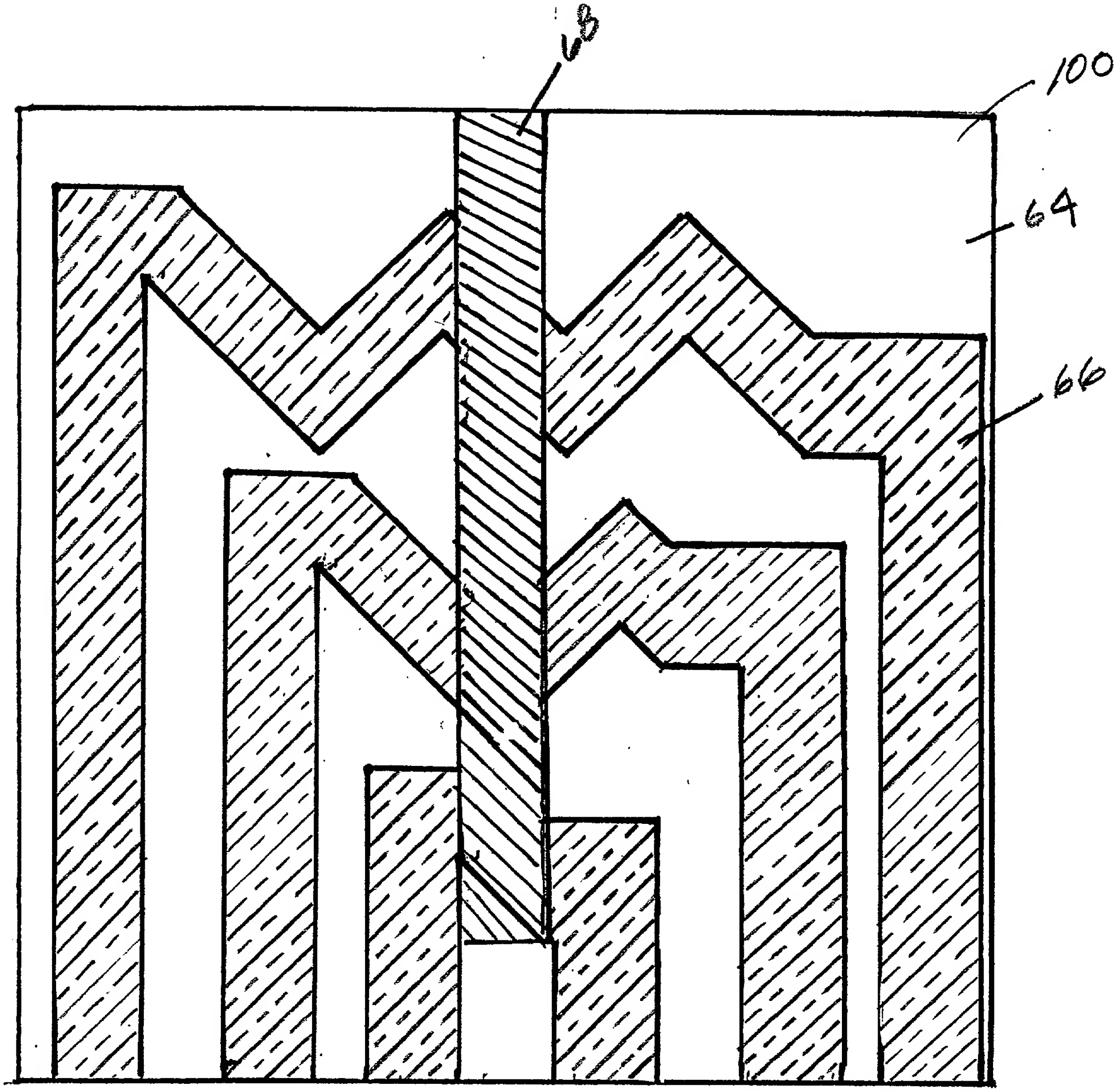

FIG. 18

DECLA .ION FOR PATENT APPLICATION (WITH POWER ATTORNEY)

As an inventor named below or on any attached continuation page, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled A METHOD AND APPARATUS FOR FORMING METAL CONTACTS ON A SUBSTRATE, the specification of which (check one):

- ☐ is attached hereto.
- ☒ was filed on September 2, 1999 as United States application serial no. 09/389,316.
- ☐ was filed on _________ as PCT international application no. _________ and was amended under PCT Article 19 on _________.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or § 365(a) of any PCT international application(s) designating at least one country other than the United States of America listed below and on any attached continuation page and have also identified below and on any attached continuation page any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America having a filing date before that of the application(s) on which priority is claimed.

Prior foreign/PCT application(s):

			Priority Claimed	
(number)	(country)	(day/month/year filed)	Yes	No
(number)	(country)	(day/month/year filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or § 365(c) of PCT international application(s) designating the United States of America listed below and on any attached continuation page and, insofar as the subject matter of each of the claims of this application is not disclosed in any such prior application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56 which became available between the filing date of such prior application and the national or PCT international filing date of this application:

(application serial no.)	(filing date)	(status - pending, patented or abandoned)
(application serial no.)	(filing date)	(status - pending, patented or abandoned)

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

(provisional application no.)	(filing date)

I hereby appoint the following Registered Practitioners to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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Salt Lake City, Utah 84110

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's signature Salman Akram Date 10/13/99
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Citizenship: Pakistan
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